GANDHI INSTITUTE OF TECHNOLOGY AND MANAGEMENT (GITAM)
(Deemed to be University)
VISAKHAPATNAM * HYDERABAD * BENGALURU

Accredited by NAAC with A^+ Grade

REGULATIONS AND SYLLABUS

OF

M.Tech. Electronics Design and Technology

(w.e.f. 2018-19 admitted batch

Department of Electrical, Electronics and Communication Engineering
GITAM (Deemed to be University)

M Tech (Electronics Design and Technology) Programme

VISION

To excel in higher education by imparting quality teaching and research and to meet the challenges in Electrical, Electronics and Communication Engineering

MISSION

1. To impart technical skills, value-based education to students, to enable them to face the demands of the industry
2. To create innovative and instructional learning methods to hone the skills for solving problems of society
3. To carry out research through constant interaction with R & D organizations and industry
4. To motivate the students to develop expertise in multidisciplinary technologies for a sustainable growth

PROGRAM EDUCATIONAL OBJECTIVES

PEO1 To impart fundamental principles and design skills in electronic/embedded systems and digital manufacturing

PEO2 To train students in using contemporary industry grade electronic design automation tools for discrete component and integrated circuit systems

PEO3 To expose students to latest developments in design of electronic systems, integrated circuits, electronic system manufacturing for pursuing research, formulating solutions to contemporary research problems of societal relevance

PEO4 To instil teamwork, leadership, and communication skills in the student with professional, ethical, and human values to be responsible citizen of the society

PROGRAMME OUTCOMES

Upon successful completion of MTech Electronics Design and Technology programme, students will be able to

PO1 apply analytical methods for design and optimization of electronic and embedded systems

PO2 analyze design analog/digital circuits and systems using analytical and graphical device models

PO3 design analog/digital systems using off-the-shelf discrete components and integrated circuit design methods balancing tradeoffs including area, power, speed and reliability

PO4 demonstrate the use of hardware equipment and software electronic design automation tools for designing analog/digital/mixed-signal electronic systems

PO5 apply research methods to formulate and solve research problems in electronic and embedded systems of contemporary relevance

PO6 describe the contemporary design challenges involved in electronic system design involving reliability, thermal and mechanical concerns

PO7 demonstrate soft skills, personality, ethics and learning enthusiasm in identifying and solving industry/research problems of contemporary relevance

PO8 survey and present state of the art electronic system design procedures for electronic system design and manufacturing

M.Tech. in Electronics Design & Technology

(in collaboration with CDAC, Hyderabad)

REGULATIONS
(w.e.f. 2018-19 admitted batch)

1. ADMISSION

1.1. Admission into M.Tech. in Electronics Design & Technology (a collaborative program of GITAM and CDAC, Hyderabad) is governed by GITAM admission regulations.

2. ELIGIBILITY CRITERIA & ADMISSION PROCEDURE

2.1. First class or equivalent grade in the qualifying examination from recognized university with a minimum of 60% aggregate marks and rank obtained in GITAM Admission Test GAT(PG).

Qualifying Examination: B.E./B.Tech/AMIE in ECE / EEE / EIE or its equivalent

2.2. Admissions into this M.Tech. programme would be on All-India basis through
- 2.2.1. Score obtained in GAT (PG), if conducted.
- 2.2.2. Performance in Qualifying Examination / Interview.

2.3. The actual weightage to be given to the above items will be decided by the authorities before the commencement of the academic year. Candidates with valid GATE score shall be exempted from appearing for GAT (PG).

3. CHOICE BASED CREDIT SYSTEM

3.1. Choice Based Credit System (CBCS) is introduced with effect from the admitted batch of 2018-19 as per UGC guidelines.

4. STRUCTURE OF THE PROGRAM

4.1. The Program Consists of

- 4.1.1. Core Engineering (CE) Courses (compulsory theory/laboratory courses) which give general exposure to a Student in Electronics Design & Technology and subject related area*.
- 4.1.2. Programme Electives (PE)*
- 4.1.3. Project Work (PW) **

* Students shall complete Core courses and Program Electives offered by GITAM (Visakhapatnam/Hyderabad Campus) in the First and Second semesters

** Student shall carry out Project work at CDAC, Hyderabad during the third and fourth Semesters. During the duration of the project work, each student shall have a main guide at CDAC, Hyderabad and a co-guide at GITAM at respective campus

4.2. Each course is assigned a certain number of credits depending upon the number of contact hours (lectures/tutorials/practicals) per week.

4.3. In general, credits are assigned to the courses based on the following contact hours per week per semester.

- One credit for each Lecture / Tutorial hour per week.
- One credit for two hours of Practicals per week.
- Two credits for three (or more) hours of Practicals per week.

5. MEDIUM OF INSTRUCTION

The medium of instruction (including examinations and project reports) shall be English.

6. REGISTRATION

Every student has to register himself / herself for each semester individually at the time specified by the Institute / University.

7. ATTENDANCE REQUIREMENTS

7.1. A student whose attendance is less than 75% in all the courses put together in any semester will not be permitted to attend the end-semester examination and he / she will not be allowed to register for subsequent semester of study. He/she has to repeat the semester along with his / her juniors.

7.2. However, the Vice Chancellor on the recommendation of the Principal / Director of the Institute / School may condone the shortage of attendance to the students whose attendance is between 66% and74% on genuine grounds and on payment of prescribed fee.

8. EVALUATION

8.1. The assessment of the student's performance in a Theory course shall be based on two components: Continuous Evaluation (40 marks) and end-semester examination (60 marks).

8.2. A student has to secure an aggregate of 40% in the course in the two components put together to be declared to have passed the course, subject to the condition that the candidate must have secured a minimum of 24 marks (i.e. 40%) in the theory component at the semester-end examination.

8.3. For courses of I & II semesters involving both Lecture and Practical component, evaluation shall be carried out with 20M (based on mid examination) + 20M (based on continuous lab evaluation) + 60M (based on end semester examination).

8.4. During the 2nd Year Project work, evaluation shall be carried out by CDAC, Hyderabad

8.5. Practical/ Project Work / Industrial Training / Viva voce / Seminar etc. courses are completely assessed under Continuous Evaluation for a maximum of 100 marks, and a student has to obtain a minimum of 40% to secure Pass Grade. Details of assessment procedure are furnished below in Table 1.

TABLE 1: ASSESSMENT PROCEDURE

S.No.	Component of Assessment	Marks Allotted	Type of Assessment	Scheme of Evaluation
1	Theory	40	Continuous Evaluation	i. Thirty (30) marks for mid Semester examinations. Three mid examinations shall be conducted for 15 marks each; performance in best two shall be taken into consideration. ii. Ten (10) marks for Quizzes, Assignments and Presentations.
		60	Semester-end Examination	i. Sixty (60) marks for Semester-end examinations
	Total	100		
2	Practicals	100	Continuous Evaluation	i. Fifty (50) marks for regularity and performance, records and oral presentations in the laboratory. Weightage for each component shall be announced at the beginning of the Semester. ii. Ten (10) marks for case studies. iii. Forty (40) marks for two tests of 20 marks each (one at the mid-term and the other towards the end of the Semester) conducted by the concerned lab Teacher.
3	Courses involving Theory and Practical Sessions	20	Continuous Evaluation	i. Twenty (20) marks for mid Semester examinations. Three mid examinations shall be conducted for 10 marks each; performance in best two shall be taken into consideration.
		20	Continuous Evaluation	ii. Twenty (20) marks for lab performance, record, regularity, case studies and end examination in the practical sessions
		60	Semester-end Examination	iii. Sixty (60) marks for Semester-end examinations
	Total	100		
4	Technical Seminar (Semester II)	100	Continuous Evaluation	i. Based on 2 Technical presentations (for 40 marks each) in the presence of a panel of examiners. These presentations shall include survey of a chosen technical topic (in the areas of Electronic Design and Packaging), simulation studies/implementation work and comparisons with related works. ii. Twenty (20) marks for overall attendance (including attendance for presentations from all the students)
5	Project work and Seminar (Semesters III and IV)	100	Continuous Evaluation	Evaluation of Project work is entirely carried out by CDAC, Hyderabad under the following guidelines: i. Forty (40) marks for periodic evaluation on originality, innovation, sincerity and progress of the work, assessed by the Project Supervisors. ii. Thirty (30) marks for mid-term evaluation for defending the Project, before a panel of examiners at CDAC, Hyderabad iii. Thirty (30) marks for final Report presentation and Viva-voce, by a panel of examiners[#] at CDAC, Hyderabad

[#] *Panel of Examiners shall be appointed by the concerned Head at CDAC Hyderabad*

9. REAPPEARANCE

9.1. A student who has secured 'F' grade in a Theory course shall have to reappear at the subsequent semester-end examination held for that course.

9.2. A student who has secured 'F' grade in a Practical course shall have to attend Special Instruction Classes held during summer.

9.3. A student who has secured 'F' Grade in Project work / Industrial Training etc shall have to improve his/her report and reappear for Viva – voce at the time of special examination.

10. SPECIAL EXAMINATION

A student who has completed his/her period of study and still has "F" grade in a maximum of three theory courses is eligible to appear for special examination.

11. BETTERMENT OF GRADES

A student who has secured only a Pass or Second class and desires to improve his/her Class can appear for betterment examinations only in Theory courses of any Semester of his / her choice, conducted along with the special examinations. Betterment of Grades is permitted 'only once' immediately after completion of the program of study.

12. GRADING SYSTEM

Based on the student performance during a given semester, a final letter grade will be awarded at the end of the semester in each course. The letter grades and the corresponding grade points are as given in Table 2.

Table 2: Grades & Grade Points

S.No.	Grade	Grade Points	Absolute Marks
1	O (outstanding)	10	90 and above
2	A+ (Excellent)	9	80 to 89
3	A (Very Good)	8	70 to 79
4	B+ (Good)	7	60 to 69
5	B (Above Average)	6	50 to 59
6	C (Average)	5	45 to 49
7	P (Pass)	4	40 to 44
8	F (Fail)	0	Less than 40
9	Ab. (Absent)	0	-

A student who earns a minimum of four grade points (P grade) in a course is declared to have successfully completed the course, subject to securing an average GPA (average of all GPAs in all the semesters) of 5 at the end of the Program to declare pass in the program. Candidates who could not secure an average GPA of 5 at the end of the program shall be permitted to reappear for a course(s) of their choice to secure the same.

13. GRADE POINT AVERAGE

A Grade Point Average (GPA) for the semester will be calculated according to the formula:

$$GPA = \frac{\sum_i C_i G_i}{\sum_i G_i}$$

Where

C_i = number of credits obtained for the i^{th} course
G_i = number of grade points obtained for the i^{th} course
To arrive at Cumulative Grade Point Average (CGPA), a similar formula is used considering the student's performance in all the courses taken, in all the semesters up to the particular point of time.

CGPA required for classification of class after the successful completion of the program is shown in Table 3.

Table 3: CGPA required for award of Class

Class	CGPA Required
First Class with Distinction	≥ 8.0 *
First Class	≥ 6.5
Second Class	≥ 5.5
Pass Class	≥ 5.0

*In addition to the required CGPA of 8.0 or more, the student must have necessarily passed all the courses of every semester in first attempt.

14. ELIGIBILITY FOR AWARD OF THE M.Tech. DEGREE

14.1. Duration of the program: A student is ordinarily expected to complete the M.Tech. programme in four semesters of two years. However a student may complete the program in not more than four years including study period.

14.2. However the above regulation may be relaxed by the Vice Chancellor in individual cases for cogent and sufficient reasons.

14.3. A student shall be eligible for award of the M.Tech. Degree if he / she fulfills all the following conditions.

a) Registered and successfully completed all the courses and projects.
b) Successfully acquired the minimum required credits as specified in the curriculum corresponding to the branch of his/her study within the stipulated time.
c) Has no dues to the Institute, hostels, Libraries, NCC /NSS etc, and
d) No disciplinary action is pending against him / her.

15. DISCRETIONARY POWER

Not with standing anything contained in the above sections, the Vice Chancellor may review all exceptional cases, and give his decision, which will be final and binding.

M.Tech. in Electronics Design & Technology

(in collaboration with CDAC, Hyderabad)

Department of Electrical, Electronics and Communication Engineering
Effective from academic year 2018-2019 admitted batch

Semester I

S. No	Course Code	Course Title	Category*	L	T	P	C
1	EDT701	Applied Maths for Manufacturing and Design	CE	3	1	2	5
2	EDT703	Analysis and Design of Analog Integrated Circuits	CE	3	1	0	4
3	EDT705	Advanced Digital System Design	CE	3	0	3	5
4	EDT707	Electromagnetic Interference and Compatibility in System	CE	3	1	0	4
5	EDT709	Advanced Embedded Systems Design	CE	3	0	3	5
6	EDTXXX	Program Elective – I	PE	3	0	3	5
7	EDT721	Electronics Design Lab	CE	0	0	4	2
8	EDT723	Analog Circuit Design Lab	CE	0	0	4	2
							32

Semester II

S. No	Course Code	Course Title	Category*	L	T	P	C
1	EDT702	Industrial Design of Electronic Products	CE	3	0	3	5
2	EDT704	MEMS and Applications	CE	3	0	0	3
3	EDT706	Design for Quality and Reliability	CE	3	0	0	3
4	EDTXXX	Program Elective –II	PE	3	1	0	4
5	EDTXXX	Program Elective – III	PE	3	1	0	4
6	EDT722	Product Design Practice and Prototyping Lab	CE	0	0	4	2
7	EDT792	Technical Seminar	CE	0	0	1	1
							22

Semester III

S. No	Course Code	Course Title	Category*	L	T	P	C
1	EDT891	Project Work and Seminar I	PW	0	0	0	8
							8

Semester IV

S. No	Course Code	Course Title	Category*	L	T	P	C
1	EDT892	Project Work and Seminar II	PW	0	0	0	12
							12

Number of Credits

Semester	I	II	III	IV	Total
Credits	32	22	8	12	74

* CE – Core Engineering, PE – Programme Elective, PW – Project Work

Programme Elective I (Choose any ONE)

S. No	Course Code	Course Title	Category*	L	T	P	C
1	EDT741	Design of Low Power Circuits	PE	3	0	3	5
2	EDT743	Semiconductor Device Modeling and Simulation	PE	3	0	3	5
3	EDT745	RF Systems Design	PE	3	0	3	5

Programme Electives II & III (Choose any TWO)

S. No	Course Code	Course Title	Category*	L	T	P	C
1	EDT742	IC Manufacturing	PE	3	1	0	4
2	EDT744	Advanced Digital Signal Processing	PE	3	1	0	4
3	EDT746	Mixed Signal Design	PE	3	1	0	4
4	EDT748	Manufacturing Engineering	PE	3	1	0	4

EDT701: APPLIED MATHS FOR MANUFACTURING AND DESIGN

L	T	P	C
3	1	2	5

Preamble:

Applied Maths for Manufacturing and Design helps in solving problems in different environments that needs decisions. The modules cover topics that include linear programming, Nonlinear programming and Integer programming, Dynamic Programming, Genetic Algorithms, and Queueing models. Analytic techniques and computer packages (MATLAB, MuPAD) will be used to solve problems facing industrial persons in decision environments.

Course Objectives:

- Mathematical modelling of any real-world problem with limited constraints and their analytical solutions using graphical method, simplex methods and using of computer packages to get solutions.
- To understand variety of problems such as assignment, transportation, etc.
- Analyse the unconstrained optimization
- Study the characteristics of dynamic programming.
- Understand the constrained and unconstrained optimization using GENETIC ALGORITHMS
- Analysed different queuing situations and find the solutions using models for different situations.

Module I **10 Hours**

Linear Programming: Introduction – formulation of the problem – graphical method – canonical form and standard forms of L.P.P – simplex method – artificial variable techniques - Big-M method – two phase simplex method. Duality principle – dual simplex method. Transportation model and algorithm, assignment model and Hungarian technique of solution, unbalanced assignment models, maximization case in transportation and assignment method. Problem solving using CPLEX

Learning Outcomes:
By the end of this Unit, the student will be able to

- Formulate the real-life problem into a mathematical model
- Solve the optimization problem graphically
- Solve the optimization problem involving in more than two decision variables using Simplex methods
- Understand the duality principle and application of dual simplex method
- Analyse the assignment and transportation problems
- Implement software packages like, MuPAD

Module II **10 Hours**

Non Linear Programming & Integer programming: Non Linear Programming: Unconstrained optimization techniques, Direct search methods, Descent methods, constrained optimization. Formulation of Integer Programming problems, Gomory's cutting plane methods, Branch and Bound Techniques. Problem solving using CPLEX

Learning Outcomes:
By the end of this Unit, the student will be able to

- Apply unconstrained optimization techniques to solve non-linear programming problems
- Understand the Golden section and Fibonacci sequence
- Explain the formulation of Integer programming

Module III **6 Hours**

Dynamic Programming: Characteristics of Dynamic Programming, Bellman's principle of optimality, Concepts of dynamic programming, tabular method of solution.

Learning Outcomes:
By the end of this Unit, the student will be able to

- Analyse the characteristics of Dynamic programming
- Follow different approaches to solve the problems
- Give/find the smallest path in the networks

Module IV **8 Hours**

Genetic Algorithm: Introduction to Genetic Algorithm (GA), working principle, coding of variables, fitness function. GA operators; Similarities and differences between GA and traditional methods; Unconstrained and constrained optimization using GAs. Problem solving using CPLEX/MATLAB

Learning Outcomes:
By the end of this Unit, the student will be able to

- Explain the terms involving in Genetic Algorithm like, parent, offspring, mutation, etc..
- Solve the constrained and unconstrained optimization problems using genetic algorithms

Module V **12 Hours**

Queuing Models: Poisson Process – Markovian queues – Single and Multi Server Models – Little's formula – Machine Interference Model – Steady State analysis – Self Service queue. Problem solving using MATLAB

Learning Outcomes:
By the end of this Unit, the student will be able to

- Explain the terms a, b, c, d, e, and e in the queue discipline (a/b/c):(d/e/f)
- Analyse steady state conditions for single server models for different queue disciplines and size of system
- Understand steady state conditions for multiple server models for different queue disciplines and size of system

Course Outcomes:

Upon completion of the courses, the student can

- be able to apply the knowledge of mathematics, basic sciences and engineering concepts along with the computer applications to solve the complex engineering problems in optimization.
- be able to design systems, components, or processes to meet appropriate needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
- Solve Linear Programming Problems
- Solve Transportation and Assignment Problems
- Identify and develop operational research models from the verbal description of the real system.
- Understand the mathematical tools that are needed to solve optimisation problems.
- Use mathematical software to solve the proposed models.
- Develop a report that describes the model and the solving technique, analyse the results and propose recommendations in language understandable to the decision-making processes in Industrial/Management Engineering.
- An ability to use the techniques, skills, and modern tools necessary for Mechanical engineering practice.
- Possess ability to estimate costs, estimate quantities and evaluate materials for design and manufacturing purposes.

EDT703: ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

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Course Objectives:

- To understand the working and modeling of NMOS and PMOS transistors.
- To analyse different single-stage MOS amplifiers, Differential amplifiers, and current mirrors.
- To devise different operational amplifier topologies using MOSFET
- To analyse and design different operational amplifiers for the given specifications
- To analyse different Op-amp Applications

Module I:

MOS transistors--large signal behaviour of MOSFET - small signal model of the MOS transistors- short channel effects in MOS transistors weak inversion in MOS transistors- substrate current flow in MOS transistor, Channel Length Modulation, Body Effect, DIBL, GIDL, Subthreshold conduction, CMOS Inverters, Voltage transfer Characteristics of CMOS inverter.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the physical structure of MOSFET (L1).
- describe the working of MOSFET in different operating regions (L2).
- estimate the second order effects in MOSFET (L2).
- model MOSFET for high frequency and low frequency operation (L4).

Module II :

Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower or Common-Drain Amplifier, Common-Gate Amplifier, Source- Degenerated, Cascode, Wilson Current Mirrors, Bipolar current Mirrors, MOS Differential Pair, Frequency Response, Band gap Reference circuits.

Learning Outcomes:

After completion of this unit, the student will be able to

- outline different amplifier configurations using MOSFET (L2).
- determine various parameters of amplifier circuits (L3).
- describe the working of differential amplifiers(L2).
- Understand the working of Current mirrors(L1)

Module III :

Noise Analysis and Operational Amplifiers: Noise- Time domain and frequency domain analysis, Noise models for circuit elements. Operational Amplifiers- Performance parameters, one stage and two stage operational amplifiers, Feedback and opamp compensation, Slew rate, Power supply rejection, Op-amp Noise.

Learning Outcomes:

After completion of this unit, the student will be able to

- distinguish between single-stage and two-stage op-amps (L2).
- analyse various parameters of operational amplifier (L4).
- illustrate the need of common-mode feedback in operational amplifiers (L3).
- understand about noise models in amplifier circuits.

Module IV:
Advanced Current Mirrors and OP-AMPS: Advanced current mirrors, Folded cascode op amp, current mirror op amp, fully differential op- amp, Common mode feedback circuits, Current feedback op-amps.

Learning Outcomes:

After completion of this unit, the student will be able to

- understand the working of Advanced current mirrors(L1)
- outline different operational amplifier topologies(L2)
- describe the working of fully differential amplifiers (L2).
- illustrate the need of common-mode feedback circuits in op amp. (L3)

Module V:
Applications of OP-AMPS: Comparators, Charge injection errors, latched comparators, CMOS and BiCMOS comparators, Sample and Hold circuits, CMOS sample and hold circuits, Bipolar and BiCMOS sample and hold circuit, switched capacitor circuits, First order filters, Biquad filters, Switched capacitor gain circuits, Continuous time filters, Gm-C filters, Bipolar, CMOS and BiCMOS Transconductors.

Learning Outcomes:

After completion of this unit, the student will be able to

- Understand the working of CMOS and BiCMOS Sample and Hold Circuits (L1)
- describe the working of Switched capacitors Circuits(L2)
- analyse various applications of operational amplifier (L4).

Course Outcomes

After successful completion of this course, the student will be able to

- understand the working and modelling of MOS transistors(L2)
- analyse different single-stage, differential amplifiers, and current mirrors(L3)
- demonstrate different single-stage and two-stage op-amp topologies(L3)
- analyse the design procedure of operational amplifiers and its performance(L4)
- able to demonstrate different Op amp applications(L3)

EDT705: ADVANCED DIGITAL SYSTEM DESIGN

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This course accustom the students with Combinational-Circuit Analysis, Combinational-Circuit Synthesis, Latches and Flip-Flops, Counters, Shift Registers, State- Machine Analysis and Design, State-Machine Synthesis, Dataflow Modeling, Behavioral Modeling, Tasks and Functions,Logic Synthesis with Verilog HDL, Test benches for verification of HDL models, Data paths and Control Units, General Data path, Timing Issues, ASM Charts,Memory, CPLDs, FPGAs and ASIC Design flow.

Course Objectives

- To understand common Combinational-Circuit Analysis and their Synthesis.
- To implement synchronous state machines using flip-flops.
- To understand the basic Concepts, modules and ports, gate level modeling, dataflow modeling, behavioral modeling and logic synthesis with Verilog HDL.
- To understand the concepts of Data paths ,Timing Issues , ASM Chats and Control Units.
- To understand the concept of Memory, CPLDs, FPGAs and ASICs.

Module I

Combinational Logic Design: Combinational-Circuit Analysis, Combinational-Circuit Synthesis, Programmed Minimization Methods, Timing Hazards, Circuit Timing, Decoders, Encoders, ThreeState Devices, Multiplexers, Exclusive-OR Gates and Parity Circuits, Comparators, Adders, Subtractors, ALUs, Combinational Multipliers

Learning Outcomes:

After completion of this unit, the student will be able to

- Explain Combinational-Circuit Analysis and Synthesis. (L2)
- Demonstrate the Programmed minimization methods, Timing hazards and Circuit Timing. (L2)
- Implementation of Combinational-Circuit and ALU. (L3)

Module II

Sequential Logic Design: Bistable Elements, Latches and Flip-Flops, Counters, Shift Registers, Clocked Synchronous State- Machine Analysis and Design, Designing State Machines Using State Diagrams, State-Machine Synthesis Using Transition Lists, State-Machine Design Example, Decomposing State Machines, Feedback Sequential Circuits, Feedback Sequential-Circuit Design

Learning Outcomes:

After completion of this unit, the student will be able to

- Design of bistable elements and sequential Circuit. (L3)
- Analysis and design of Clocked Synchronous State- Machine. (L5)
- Design of Feedback Sequential-Circuit. (L3)

Module III

Verilog HDL: Overview of Digital Design with Verilog HDL, Hierarchical Modeling Concepts, Basic Concepts, Modules and Ports, Gate Level Modeling, Dataflow Modeling, Behavioral Modeling, Tasks and Functions, Useful Modeling Techniques, Timing and Delays, User Defined Primitives, Logic Synthesis with Verilog HDL, Test benches for verification of HDL models

Learning Outcomes:

After completion of this unit, the student will be able to

- Describe basic concepts, Modules and Ports, Gate level modeling, dataflow Modeling, behavioral modeling. (L3)
- Analyze timing and delays, logic synthesis with verilog HDL, test benches for verification of HDL models. (L5)

Module IV

Data paths and Control Units: Designing Dedicated Data paths, Using Dedicated Data paths, Examples of Dedicated Data paths, General Data paths, Using General Data paths, A More Complex General Data path, Timing Issues, Constructing the Control Unit, Examples, Generating Status Signals, Timing Issues, Standalone Controllers: Rotating Lights and PS/2 Keyboard Controller, ASM Charts and State Action Tables Suggested activities: Dedicated Microprocessor and General-Purpose Microprocessor Design

Learning Outcomes:

After completion of this unit, the student will be able to

- Explain dedicated data paths, General Data paths. (L2)
- Describe more complex general data path, timing issues, constructing the control Unit. (L3)
- Implementation of ASM charts and state action tables. (L3)

Module V

Memory, CPLDs, FPGAs and ASICs Read-Only Memory, Read/Write Memory, Static RAM, Dynamic RAM, Complex Programmable Logic Devices, Field-Programmable Gate Arrays, Types of ASICs, ASIC Design flow, Economics of ASICs

Learning Outcomes:

After completion of this unit, the student will be able to

- Explain memory, Read/Write memory, Static RAM, Dynamic RAM. (L2)
- Demonstrate Complex Programmable Logic Devices and Field-Programmable Gate Arrays. (L3)
- Describe the types of ASICs and ImplementationASIC Design flow. (L4)

Text Books

1. John F. Wakerly, “Digital Design: Principles and Practices”, 4th edition, Pearson, 2008
2. Charles Roth, Lizy Kurian John, Digital System Design with Verilog, Cengage Learning, 2015.
3. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd edition, Pearson, 2003
4. Enoch O.Hwang, “Digital Logic and Microprocessor Design with VHDL”, 1st edition, Nelson Engineering, 2007

References:

1. Michael John Sebastian Smith, “Application-Specific Integrated Circuits”, 1st edition, Pearson, 2002
2. Charles H. Roth, “Fundamentals of Logic Design”, 5th edition, Cengage Learning, 2004
3. Randy H.Katz, Gaetano Borriello, “Contemporary Logic Design”, 2nd edition, Prentice Hall of India Learning, 2009

Course Outcomes:

After successful completion of the course, the student will be able to

- Understand the fundamental concepts of Combinational-Circuit Analysis and Synthesis and designing of Combinational-Circuit and ALU. (L4)
- Develop competence in analysis of synchronous and asynchronous sequential circuits and Analyze and solve various engineering problems with finite state machines. (L5)
- Describe Verilog HDL model for combinational and sequential circuits and test pattern generation. (L3)
- Understand datapaths, general data paths, timing issues, constructing the control Unit. (L3)
- Study of memory, Read/Write memory, Static RAM, Dynamic RAM. (L2)
- Describe CPLD,FPGA and Implementation ASIC Design flow. (L5)

EDT707: ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM

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Course Description:
Electromagnetic Pollution is a major concern in today's world. This course is designed for understanding Electro Magnetic Interference and to provide knowledge related to sources of EMI and aspects of EMC measurements about radiated emissions, conduction emissions, radiated susceptibility and conduction susceptibility are necessary to know about radiation levels. This course focuses on understanding the concept of coupling mechanisms of EMI and immunity to conducted EMI and EMC standards.

Course Objectives:

- To understand the concepts of electro-magnetic interference and electro-magnetic compatibility.
- To impart the knowledge of sources of EMI and their constraints.
- To illustrate concepts of EMC measurements.
- To understand the concepts of EMI problems and their solution methods in PCB level and system level design.
- To Understand the concepts PCB tracing and implementation with EMC constraints.

Module I **9 Hours**

Fundamentals and Requirements: Introduction to EMC, EMC problem classifications, Physical and electrical dimensions of components, Common EMC units, Transmission line theory, EMC signal sources EMC standards, conducted emissions standards and testing, Radiated emissions standards and testing, Antenna factor, Regulations: FCC and CISPR

Learning Outcomes:
After completion of this module, the student will be able to

- state the concept of electromagnetic environment. (L1)
- illustrate about sources of EMI and their constraints. (L1)
- describe EMC standards. (L2)
- illustrate concepts of EMC measurements. (L2)

Module II **9 Hours**

Component Behavior: Low frequency circuit approximations, Internal impedance of round wires, High frequency wire resistance approximation, External inductance, capacitance and conductance of parallel wires, coaxial conductors and PCB structures, non-ideal behavior of resistors, capacitors and inductors, Noise suppression with capacitors and inductors, Common mode and differential mode currents, Ferrites and common mode chokes, Digital Circuit Devices

Learning Outcomes:

After completion of this module, the student will be able to

- diagnose and solve basic electromagnetic compatibility problems. (L3)
- analyze how electromagnetic noise couples to an electrical system. (L2)
- describe the methods, how electromagnetic noise suppressed in an electrical system. (L3)
- can estimate the emission levels for simple circuits. (L4)

Module III **9 Hours**

Signal Spectra and Radiated Emission & Susceptibility: Signal classifications - Periodic signals as series expansions of orthogonal basis functions, Fourier series, Signal spectra, Efficient techniques for the determination of Fourier series coefficients, Fourier expansions of piecewise linear periodic signals, Approximate spectra of digital circuit clock waveforms, Aperiodic signals, Fourier transforms, Linear systems response to periodic and aperiodic signals. Emission models for wires and PCB lands, Signal spectra and the spectra of resulting radiated emissions, Measured spectra and the effect of antenna factor

Learning Outcomes:
After completion of this module, the student will be able to

- compute the Fourier series and Fourier Transform for periodic and aperiodic signals (L2).
- knows and can use models of basic elements at high frequency. (L3)
- evaluate the emission, immunity level from different systems and antenna to couple with the prescribed EMC standards. (L4)

Module IV **9 Hours**

Crosstalk, Shielding and EMC/EMI Modelling: Crosstalk on three-conductor transmission lines, multi-conductor transmission line per-unit-length parameters, electrically short, weakly-coupled three-conductor line, Common-impedance coupling, Time-domain crosstalk Far-field shielding effectiveness, Near-field shielding effectiveness, EMC/EMI Computational Modelling: Importance of modelling, FDTD and Methods of Moments Techniques.

Learning Outcomes:
After completion of this module, the student will be able to

- describe the Grounding, Shielding, Bonding mechanisms for EMC. (L2).
- understand the mechanism of EMI emission/coupling in transmission lines. (L3)
- analyse the crosstalk in transmission lines. (L5)

Module V **9 Hours**

EMC Design of PCBs and Electro Static Discharge: PCB: Board Stack-up Issues, Component Placement, Isolation. Electro Static Discharge (ESD): Dielectric Breakdown, Static Charge Generation, Human Body Model, Static Discharge, ESD Protection

Learning Outcomes:
After completion of this module, the student will be able to

- explain the causes and types of static electricity. (L1)
- able to handle Electrostatic Discharge Sensitive equipment appropriately. (L3)
- Understand the PCB stack-up design to minimize radiation and decrease crosstalk problems on high-speed systems. (L5)
- Explain the PCB layout design to improve the electromagnetic compatibility. (L4)

Text Books:

1. Clayton R. Paul, "Introduction to Electromagnetic Compatibility", 2/e, John Wiley and Sons, 2006.
2. Henry W Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, 2/e, 1988.
3. Bruce R Archambeault, "PCB Design for Real-World EMI Control", Springer Science and Business Media, LLC, 2002.

Course Outcomes:

After completion of course the student shall be able to:

- CO1. Give examples on how electromagnetic Interference is generated in large and small electrical systems. (L2)
- CO2. Show theoretically how electromagnetic noise couples to an electrical system. (L3)
- CO3. Derive the frequency domain and time domain representation of signals using transform techniques for emission models. (L4)
- CO4. Explain how electromagnetic noise can be reduced in an electrical system using proper layout, shielding, grounding, and filtering. (L3)
- CO5. Describe and give practical examples of the problem of electromagnetic interference. (L5)

EDT709: ADVANCED EMBEDDED SYSTEMS DESIGN

L T P C

3 0 3 5

This course emphasizes on comprehensive treatment of embedded hardware and real time operating systems along with communication protocols that are required in Embedded Systems development. Memory and I/O interfacing concepts are also elaborated for giving deep knowledge about system development. Advanced microcontrollers and their applications are also introduced to the students.

Course Objectives:

- To introduce the embedded hardware and embedded system evolution trends to the students
- To study the basic concepts of Real Time Operating Systems
- To get familiarized with advanced microcontrollers and their applications
- To gain knowledge about serial and parallel communication protocols that are used in embedded system development
- To understand the concepts of memory and input/output devices interfacing with the processor

Module I 8 Hours

Introduction and Review of Embedded Hardware: Terminology - Gates - Timing diagram - Memory - Microprocessor buses - Direct memory access Interrupts – Built interrupts - Interrupts basis - Shared data problems - Interrupt latency – Embedded system evolution trends - Round robin- Round robin with interrupt function Rescheduling architecture - algorithm.

Learning Outcomes:

- After completion of this unit, the student will be able to
- Recall the basic concepts of Embedded System hardware (L1)
- Outline the Embedded System evolution trends (L2)
- Summarise the basic concepts of scheduling (L2)

Module II 10 Hours

Real Time Operating System: Task and Task states - Task and data - Semaphore and shared data, operating system services - Message queues timing functions - Events - Memory management - Interrupt routines in an RTOS environment - Basic design using RTOS.

Learning Outcomes:

- After completion of this unit, the student will be able to
- Outline the basic concepts of Real Time Operating System (L2)
- Summarise the Operating Systems Services (L2)
- Interpret the memory management techniques (L2)
- Apply the basic design methods of RTOS (L3)

Module III 9 Hours

Advanced Processors/Controllers: Introduction to ARM CPU Architecture, Programmers Model for ARM CPU, Operating Modes, Instruction set, ARM Exception Handling, Pipelining, Comparative Study of ARM cores – ARMv4 to ARM Cortex

Learning Outcomes:

- After completion of this unit, the student will be able to
- Summarize the architectural features of the ARM CPU (L2)
- Select appropriate controller for implementation (L3)
- List out various features and applications of ARM variants (L4)
- Choose appropriate instruction to write a program for ARM (L5)

Module IV 9 Hours

Embedded Hardware, Software And Peripherals: Peripheral-Processor Interfacing Concepts - Review of Peripheral Interface protocols - SPI, I2C, UART and One-wire with case studies of interface with Sensors, Radio and ADCs. Hardware Timers and Interrupt handling, Interrupt service routines. Software Development environment.

Learning Outcomes:
After completion of this unit, the student will be able to

- Demonstrate the interfacing of peripherals to the processor (L2)
- Make use of Serial Communication Protocols in Embedded System Design (L3)
- Utilize the timers in generating the interrupts (L3)

Module V 9 Hours

Memory and Interfacing: Memory: Memory write ability and storage performance - Memory types - composing memory- Advance RAM interfacing communication basic - Microprocessor interfacing I/O addressing Interrupts - Direct memory access – Arbitration multilevel bus architecture - Serial protocol, Parallel protocols - Wireless protocols - Digital camera example.

Learning Outcomes:
After completion of this unit, the student will be able to

Illustrate the difference between different types of memories (L2)
Show how the memory can be interfaced to the processor (L2)
Organize multiple processors in the Embedded system development (L3)
Categorize different protocols used in interfacing the processor with the peripherals (L4)

Textbooks

1. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.
2. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006. 3. Andrew N Sloss, “ARM System Developers Guide”, Elsevier, 2013

References

1. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons, 2002.
2. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.
3. Tammy Noergaard, ”Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2006
4. Michael Barr, “Programming Embedded Systems in C and C++”, O'Reilly, 1999

Course Outcomes:
After successful completion of the course, the student will be able to

- Summarise the basic concepts of Embedded System hardware and RTOS (L2)
- Apply the basic design methods of RTOS in developing an Embedded System (L3)
- Choose appropriate instruction to write a program for ARM (L5)
- Make use of Serial Communication Protocols in Embedded System Design (L3)
- Appraise the working of various functional units in a complex Embedded System (L5)

EDT721: ELECTRONICS DESIGN LAB

L T P C
0 0 4 2

Tools and Equipment needed:
Hand held Digital Multimeter (AC/DC Range : 500μA to 10A, 50 mV to 100V), Analog Oscilloscope(0-20MHz, 2-Channels), Mixed Signal Oscilloscope(0-1GHz, 16 channels), Digital Oscilloscope(0-100MHz, 4-Channels, upto 2Gs/S Sample rate), Function Generator (0-80MHz, sine and square waveforms, 64 K point arbitrary waveforms), Pulse Generator(0-10MHz, Squarewave, double pulse & delayed pulse modes), DC power supply(0 to +30V, 0 to 5A), Prototyping Board(Microcontroller and FPGA based boards), PCB Design Tools- CADSTAR, Cadence Allegro etc, ESD Safe Lab Table and chairs with mats and equipment, Soldering and de-soldering equipment and tools with consumables, Various Heat sinks, Cooling fans for electronic equipment.

Lab Experiments:

1. **PCB Design** **(30 Hrs.)**
    1. Artwork & printing of a simple PCB, Double Sided PCB
    2. Etching & drilling of PCB
    3. PCB Design with Design rules using CAD packages
    4. Mounting and soldering of component with protection of ESD
    5. Testing of regulated power supply fabricated
    6. Design of Heat-sink with cooling system
    7. Wire-harnessing and case study of Wire-harness in SMPS and dual power supplies
    8. Fabricate and test the audio amplifier circuit, music system by using above power supply

2.**DC and AC Measurements:** **(9 Hrs.)**
1. To get familiar with use of Digital Multimeter, DC power supplies, oscilloscope, function generator and pulse generator.
2. To measure different time varying electrical signals with respect to : DC and AC voltages, Frequency, Phase, Time constant of RC circuit , Amplitude and phase shift responses of low pass and high pass RC filter using the necessary equipment and prototyping boards.

3.**Optoelectronics:** **(9 Hrs.)**
To get familiar with the use of Light Emitting Diodes (LEDs), LASER diodes, light sensors (Photo diodes, Photo transistors) with the aid of different equipment such as Digital Oscilloscope, Pulse Generator, DC power supply and prototyping board.

4.**Electronic System Issues:** **(12 Hrs.)**
Cabling of Electronic Systems:
Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables.

Grounding of Electronic Systems: Safety grounds, signal grounds, single-point ground systems, multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies.

Protection against Electro-Static Discharges (ESD):
Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC.

Cooling in/of Electronic System: Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection.

Text Books

1. Kim R. Fowler, "Electronic Instrument Design", 1/e, Oxford University Press, 1996.
2. Henry W. Ott, "Noise Reduction Techniques in Electronic Systems", 2/e, John Wiley and Sons, 1988.
3. John F. Wakerly, "Digital Design Principles and Practices", 3/e, Prentice Hall International, 2016.
4. Robert F. Coughlin, "Operational Amplifiers and Linear Integrated Circuits", 3/e, Prentice Hall International, 2001.

References

1. William Bosshart, "Printed Circuit Boards - Design & Technology", 1/e, Tata McGraw Hill, 1983.
2. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies; Application note SDAA011A@ http://www.ti.com
3. PCB Design Guidelines For Reduced EMI; Application note SZZA009@http://www.ti.com

EDT723: ANALOG CIRCUIT DESIGN LABORATORY

L T P C
0 0 4 2

Course Description:
Analog circuit design laboratory course is designed to cater to the needs of industry for high performance analog design. The course focuses on design, analysis and optimization techniques and practicing those for analog circuit design.

Tools used:
LTSpice, Electric EDA tool, Cadence EDA tool suite (Virtuoso ADE, Spectre, Assura DRC)

Course Objectives:

- To impart the knowledge of MOS Transistor operation and characterization
- To impart the knowledge of single stage amplifiers and their design and analysis
- To explore the optimization techniques for optimizing the performance of single stage amplifiers
- To understand the design approaches of multi-stage amplifiers, such as two-stage operational amplifier and explore compensation techniques
- To understand performance enhancement techniques for optimizing the performance of Op-Amp, such as Folded Cascode topology, Current mirror Op-Amp, Fully differential Op-Amp, Current feedback topology, and CMFB
- To impart knowledge on biasing techniques for MOS amplifiers, such as Current mirrors like Wilson current mirror, and Bandgap reference circuit
- To understand design approaches of Comparators, Switched Capacitor circuits, Sample and hold circuits, and Active filters
- To design layout for all the circuits and to perform LVS, perform Parasitic extraction

I. Spice Analysis of Basic circuits - 5 hrs

1. Layout and simulating the I-V curves of PMOS and NMOS devices.
2. Design, Layout and Simulation of CMOS inverter.
3. Design, Layout and Simulation of CMOS NAND gate.
4. Design, Layout and Simulation of Ring Oscillator.

Learning Outcomes:
After completion of this module, the student will be able to

- Quantify the performance of MOSFETs
- Construct Complementary MOS logic circuits and identify the operating region for high gain
- Construct single ended Ring oscillators and quantify their performance

II. Case studies on spice Analysis of MOS amplifiers - 10 hrs

1. Estimation of small signal voltage gain and frequency plot of Common Source Amplifier.
2. Estimation of small signal voltage gain and frequency plot of Common Drain Amplifier/Source Follower.
3. Estimation of small signal voltage gain and frequency plot of Common Gate Amplifier.
4. Estimation of small signal voltage gain and frequency plot of Common Source Amplifier with source degeneration.
5. Estimation of small signal voltage gain and frequency plot of Common Source Amplifier with compensation network.

6. Estimation of small signal voltage gain and frequency plot of Cascode Amplifier.
7. Estimation of small signal voltage gain and frequency plot of basic Differential Amplifier.

Learning Outcomes:

After completion of this module, the student will be able to

- Design and analyze Single stage amplifiers-Common Source (CS), Common Gate(CG) and Common Drain (CD) configurations
- Analyze how source degeneration effects the performance of CS amplifier
- Describe the frequency compensation methods, and illustrate its application for the frequency compensation of CS amplifier
- Design Cascode (CS-CG) amplifier and analyze its performance
- Design Differential amplifier and to perform small signal and AC analysis

III. Case studies on design of Current mirrors and Band-Gap reference circuits- 5 hrs

1. Simulation and analysis of a basic Current mirror circuit.
2. Simulation and analysis of Wilson current mirror circuit.
3. Simulation and analysis of a bipolar current mirror circuit.
4. Simulation and analysis of a CMOS Band-gap reference circuit.

Learning Outcomes:

After completion of this module, the student will be able to

- Design and simulate basic current mirror circuit and other high performance current mirrors (Wilson current mirror and Bipolar current mirror)

Design and simulate CMOS Band-gap reference circuit

IV. Case studies on spice Analysis of Operational Amplifiers- 5 hrs

1. Design, Frequency plot and analysis of a single stage op-amp.
2. Design, Frequency plot and analysis of a two stage op-amp.
3. Design, Frequency plot and analysis of a two stage op-amp with compensation network.

Learning Outcomes:

After completion of this module, the student will be able to

- Design and simulate Single-stage Op-Amp and quantify its performance
- Design and simulate Two-stage Op-Amp and quantify its performance
- Design frequency compensation network for the given specifications, and quantify the performance of Op-Amp with compensation

V. Case studies on spice Analysis of Advanced current mirrors and Operational Amplifiers-15 hrs

1. Simulation and analysis of a wide swing current mirror circuit.
2. Simulation and analysis of a wide swing current mirror circuit with enhanced output impedance.
3. Design, Frequency plot and analysis of a folded cascode op-amp.
4. Design, Frequency plot and analysis of a current mirror op-amp.
5. Design, Frequency plot and analysis of fully differential op-amp.
6. Design, Simulation and analysis of common mode feedback circuit(CMFB).
7. Design, Frequency plot and analysis of current feedback op-amp.

Learning Outcomes:

After completion of this module, the student will be able to

- Explore the concept of current mirrors, and design wide swing current mirror circuits
- Design and simulate Folded-Cascode Op-Amp and quantify its performance
- Design and simulate Current mirror Op-Amp and quantify its performance

- Design and simulate Fully differential Op-Amp and quantify its performance
- Explore CMFB and its application for designing Op-Amps
- Design and simulate Current feedback Op-Amp and quantify its performance

6.Case studies on design of Comparators, Sample and Hold circuits, Switched capacitor circuits, etc **20 hrs**

1. Design, Simulation and analysis of a basic comparator.
2. Design, Simulation and analysis of a high speed comparator (latched comparator).
3. Design, Simulation and analysis of an open loop track and hold using MOS technology.
4. Design, Simulation and analysis of Sample and Hold circuit with clock feedthrough circuitry.
5. Design, Simulation and analysis of basic switched capacitor circuit.
6. Design, Simulation and analysis of discrete time integrator circuits (parasitic sensitive and insensitive).
7. Design, Simulation and analysis of first order RC filter circuit.
8. Design, Simulation and analysis of low Q and high Q biquad filters.
9. Design, Simulation and analysis of first order Gm-C filter circuit.

Learning Outcomes:

After completion of this module, the student will be able to

- Explore the concept of basic comparators, and design and simulate comparator circuits
- Design and simulate high-speed comparator and quantify its performance
- Design and simulate Sample-and-hold circuit (or Track and hold) and quantify its performance
- Design and simulate Switched Capacitor filters and amplifiers
- Explore design approaches for active filters using Op-Amps and RC circuits

Course Outcomes:

After completion of course the student shall be able to:

1. Demonstrate the operation of Single stage amplifiers and design for given specifications
2. Demonstrate the operation of Operational amplifiers and design for given specifications
3. Demonstrate the operation of basic Current mirrors and high swing current mirrors and design for given specifications
4. Demonstrate the operation of high-performance Op-Amps and design and analyze for given specifications
5. Design and simulate high-speed comparators and Switched capacitor filter circuits, and characterize them

Text Books

1. David A. Johns and Ken Martin, “Analog Integrated Circuit Design”, 2/e, Oxford University Press, 2010.
1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, 2/e, Tata McGraw Hill, 2016.
2. Jan Rabaey, “Low Power Design Essentials”, Springer Edition, 2009.

References

1. Phillip E. Allen, Douglas R. Hollberg, “CMOS Analog Circuit Design”, 2/e, Oxford University Press, 2003.
2. Gray, Meyer, Lewis, Hurst, “Analysis and Design of Analog Integrated Circuits”, 5/e, Willey India Private Limited, 2015.

EDT741: DESIGN OF LOW POWER CIRCUITS

L	T	P	C
3	0	3	5

Course description:

The increasing prominence of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density chips have led to rapid and innovative developments in low-power design during the recent years. This course is designed for understanding various types of power dissipations in CMOS Circuits and how to design the circuits for low power dissipation.

Course Objectives:

At the end of the course, the student should be able to

- Explain the MOS transistor structure & modelling of MOS Transistor
- Illustrate Different logic families
- Understand types of power dissipation and differentiate various types of Power dissipation
- Understand the concept of supply voltage scaling approach
- Explain switched capacitance Minimization approaches
- Explain leakage power minimization approaches

Module I **9 Hours**

Basics of MOS circuits: MOS Transistor structure and device modelling, MOS Inverters, MOS Combinational Circuits, Different Logic Families

Learning Outcomes:

At the end of this module, the student will be able to

- Understand the MOS transistor structure(L3)
- Analyze MOS inverter and MOS Combinational circuits(L5)
- Illustrate various logic families(L2)

Module II **9 Hours**

Sources of Power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power, Glitching Power. Static Power Dissipation, Degrees of Freedom

Learning Outcomes:

At the end of this module, the student will be able to

- Understand the types of power dissipation(L2)
- Define &derive static, dynamic & switching power dissipations(L2)
- Compute the power dissipation for the given circuit(L4)

Module III **9 Hours**

Supply Voltage Scaling Approaches: Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management.

Learning Outcomes:

At the end of this module, the student will be able to

- Understand the concept of MOS transistor scaling(L2)

- Understand architectural level approaches, parallelism, pipelining (L2)
- Understand Dynamic voltage frequency scaling(L2)

Module IV **9 Hours**

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff, Bus Encoding, Two's complement Vs Sign Magnitude, Architectural optimization, Clock Gating, Logic styles

Learning Outcomes:

At the end of this module, the student will be able to

- Analyze hardware, software co design & tradeoffs(L5)
- Explain various bus encoding techniques(L2)
- Understand the concept of clock gating(L2)

Module V **9 Hours**

Leakage Power Minimization Approaches: Variable threshold voltage CMOS (VTCMOS) approach, multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-V_t assignment approach (DTCMOS). Adiabatic Switching Circuits, Battery-aware Synthesis, Variation tolerant design, CAD tools for low power synthesis

Learning Outcomes:

At the end of this module, the student will be able to

- Understand various concepts of leakage power minimization techniques(L2)
- Design circuits by including leakage power reduction techniques(L6)
- Understand the concept power gating. Adiabatic switching(L2)
- Design adiabatic switching circuits(L6)

Text Books

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, 3/e, Tata Mcgraw Hill, 2003.
2. Neil H. E. Weste, K. Eshraghian, Principles of CMOS VLSI Design, 2/e, Addison Wesley Indian reprint, 1993.
3. A. Bellamour, M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995.
4. Anantha P. Chandrakasan, Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.

Course Outcomes:

At the end of the course, the student should be able to

- Explain the MOS transistor structure & modeling of MOS Transistor(L2)
- Illustrate Different logic families(L2)
- Understand types of power dissipation and differentiate various types of Power dissipation(L3)
- Implementations of supply voltage scaling approach(L6)
- Explain switched capacitance Minimization approaches(L2)
- Explain leakage power minimization approaches(L2)

EDT743: SEMICONDUCTOR DEVICE MODELING AND SIMULATION

L	T	P	C
3	0	3	5

Module I **9 Hours**

PN Junction Diode and Schottky Diode: DC Current- Voltage Characteristics, Static Model, Large- Signal Model, Small- Signal Model, Schottky Diode and its implementation in SPICE2, Temperature and Area Effects on the Diode Model Parameters, SPICE3 Models, HSPICE Models, PSPICE Models

Module II **9 Hours**

Bipolar Junction Transistor (BJT): Transistor Conversions and Symbols, Ebers-Moll Static Model, Ebers-Moll Large Signal Model, Ebers-Moll Small Signal Model, Gummel-Poon Static Model, Gummel-Poon Large Signal Model, Gummel-Poon Small Signal Model, Temperature and Area Effects on the BJT Model Parameters, Power BJT Model, SPICE3 Models, HSPICE Models, PSPICE Models

Module III **6 Hours**

MOS Transistor(MOST) Theory: Introduction, Long-Channel I-V Characteristics, C-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics

Module IV **11 Hours**

MOS Transistor Models: LEVEL 1 Static Model, LEVEL 2 Static Model, LEVEL 1 and LEVEL 2 Large-Signal Model, LEVEL 3 Static Model, LEVEL 3 Large-Signal Model, Comments on the Three Models, The Effects of Series Resistances, Small-Signal Models, The Effect on Temperature on the MOST Model Parameters, BSIM1 Model, BSIM2 Model, SPICE3 Models, HSPICE Models, PSPICE Models

Module V **10 Hours**

MOS Transistor Parameter Measurements: LEVEL1 Model Parameters, LEVEL2 Model (Long-Channel) Parameters, LEVEL2 Model (Short- Channel) Parameters, LEVEL3 Model Parameters, Measurements of Capacitance, BSIM Model Parameter Extraction

Text Books

1. Giuseppe, Massobrio, “Semiconductor Device Modeling with SPICE”, 2/e, Tata McGraw Hill, 1998.
2. Yannis P. Tsividis, Colin Mc Andrew, “Operation and Modeling of the MOS Transistor”, 2/e, Oxford University Press, 2011.

References

1. B. G. Streetman, S. Banerjee, “Solid State Electronic Devices”, 6/e, Prentice Hall of India Learning, 2015.
2. S. M. Sze, “Semiconductor Devices: Physics and Technology”, 2/e, Wiley India Pvt Ltd, 2008
3. Michael Shur, “Physics of Semiconductor Devices”, 3/e, Wiley India Pvt Ltd, 1990.
4. Nandita Das Gupta, Amitava Das Gupta, “Semiconductor Devices”, 1/e, Prentice Hall of India Learning Private Limited, 2004.
5. Karl Hess, “Advanced Theory of Semiconductor Devices”, 1/e, IEEE Computer Society Press, 2000.

EDT745: RF SYSTEMS DESIGN

L T P C
3 0 3 5

Module I **9 Hours**

CMOS physics, transceiver specifications and architectures CMOS: Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise, Specification distribution over a communication link Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures, Transmitter: Direct up conversion, Two step up conversion, Printed antennas.

Module II **9 Hours**

Impedance Matching and Amplifiers: S-parameters with Smith chart, Passive IC components, Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design. Low Noise Amplifiers: Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

Module III **9 Hours**

Feedback Systems and Power Amplifiers: Feedback Systems: Stability of feedback systems: Gain and phase margin, Root locus techniques, Time and Frequency domain considerations, Compensation Power Amplifiers: General model, Class A, AB, B, C, D, E and F amplifiers, linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

Module IV **9 Hours**

PLL and Frequency Synthesizers: PLL Linearized Model, Noise properties, Phase detectors, Loop filters and Charge Pumps Frequency Synthesizers: Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

Module V **9 Hours**

Mixers and Oscillators: Mixer Characteristics, Non-linear based mixers: Quadratic mixers, Multiplier based mixers. Single balanced and double balanced mixers, sub-sampling mixers. Oscillators: Describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

Text Books

1. Thomas Lee, “Design of CMOS RF Integrated Circuits”, 2/e, Cambridge University Press, 2004.
2. Behzad Razavi, “RF Microelectronics ”, 2/e, Pearson Education, 2001.
3. Debatosh Guha, Yahia M MAntar, “Microstrip and Printed Antennas: New Trends, Techniques and Applications”, Wiley Publications, 2011.

References

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, 4/e, Wiley India Student Edition, 2001.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, 2/e, Mc Graw Hill Publications, 2016.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. Rod Waterhouse, “Printed Antennas for Wireless Communications”, Wiley, 2007.

EDT702: INDUSTRIAL DESIGN OF ELECTRONIC PRODUCTS

L	T	P	C
3	0	3	5

Course Description:
This course is intended to prepare students to design products based on product design principles, guidelines and skills. Students will be given experience of designing products through case studies. At the end of the course students will communicate design concepts through sketches, virtual and physical appearance model.

Course Objectives:

- To understand the various processes and systems to address human needs by creating tangible Electronic Products.
- Students able to learn to communicate and present their design ideas by applying visual communication techniques such as sketching, rendering.
- To pursue learners with emphasis on learning-by-doing and following a comprehensive process of design, engineering and producing products and systems.
- To understand the concepts of using ergonomic principles to recognize, evaluate and control workplace conditions that cause or contribute to musculoskeletal and nerve disorders.
- To enable the students to design electronic products with planning/production and layouts design concepts.

Module I **12 Hours**

Introduction to Industrial Design: Introduction to the course, role of ID in the domain of industry, product innovation, Designer's philosophy and role in product design, what is good design. **Product Design Methodology:** User Centered Design methods, Systems Approach, Electronic Product Design and Development Methodology, Design Thinking, Creativity and Innovation. Introduction to Sustainable Design. Design Case Studies.

Learning Outcomes:
After completion of this module, the student will be able to

- understand the role of Industry design. (L1)
- describe the concepts of electronic product design and development methodologies. (L2)
- know, how to approach innovation challenges from a human-centered perspective. (L3)

Module II **9 Hours**

Deconstructing Product Design: Product Analysis. Visual Communication Techniques**:** Free Hand sketching and drawing techniques for concept presentation, Perspectives, and rendering techniques, color in design, Engineering drawing practice, exploded views.

Learning Outcomes:
After completion of this module, the student will be able to

- demonstrate understanding of skills in fundamental visual communication techniques. (L2)
- demonstrate understanding of skills in drawing techniques to communicate complex and detailed visual information. (L3)
- the ability to create visual representations through applying basic visual communication principles in layout and typography to better organize and visually structure the information. (L3)

Module III **10 Hours**

Design Principles: Visual information through design principles, Figure-ground relationship, Visual information distribution, Gestalt principles, Theory of object perception, Symmetry, Asymmetry, Closure, Continuance, Unifying principles of design. Design Expressions: Mood board, Design trends, Application of design principles and product aesthetics.

Learning Outcomes:

After completion of this module, the student will be able to

- understand the concept of figure-ground relationship. (L2)
- understand the concept of Gestalt principles. (L2)
- demonstrate an understanding of the aesthetics of form development and of the history and current state of design. (L5)

Module IV **9 Hours**

Ergonomics: Ergonomics of electronic products and systems, Control panel design, User interface design, Human-Computer Interaction, Case studies.

Learning Outcomes:

After completion of this module, the student will be able to

- understand the scope of ergonomics and the application of ergonomic principles to workplace design and work organization. (L2)
- describe and apply the principles of good ergonomic design of work areas and equipment to a range of occupational settings. (L4)
- apply Ergonomic principles to decrease the strain on a human body allowing them to work harder or for longer while remaining comfortable and avoiding injury. (L5)

Module V **9 Hours**

Product Engineering: Product architecture, Layout design, Structure design. Product detailing in sheet metal and plastics for ease of assembly, maintenance and aesthetics. Electronic Product Design Project / Problem Solving / Re-Design.

Learning Outcomes:

After completion of this module, the student will be able to

- apply the layout and structure design concepts to design a product architecture. (L2)
- *Analyze an* importance of creating and testing prototypes during the engineering *design* process. (L4)

Text Books

1. Peter Z., “German Design Standard Vol 2”, Reddot, 2006.
2. Clarkson P.J, Coleman R. and Keates, S., “Inclusive Design, Design for the whole population”, Springer Verlag Gmbh, 2003

3. Jordan P. W., "Designing Pleasurable Products: An Introduction to the New Human Factors." Taylor and Francis, 2002.
4. Otto K.and Wood K., "Product design: Techniques in Reverse Engineering and New Product development ", Prentice Hall, 2001.
5. Cross N. "Engineering Design Methods: Strategies for Product Design", Wiley, 2000.

References

1. Cagan J.and Vogel C. M., Creating Breakthrough Products, "Innovation from Product Planning to Program Approval" . Pearson Education, 2007.
2. Coats D. , "Watches Tell More than Time: Product Design, Information, Quest for elegance" McGraw Hill, 2002
3. Norman D. A. , "The design of everyday things, Basic Books, 2002.
4. Chakrabarty D., "Indian Anthropometric Dimensions for Ergonomic Design Practice", NID, Ahmedabad, 1999.
5. Kelley T. and Littman J. "The Art of Innovation: Lessons in Creativity from Ideo, America's Leading Design Firm, Doubleday", Ver: 4 November 2011.
6. E.J. Mc Cormic, Human factors in engineering design, McGraw Hill, 1976

Journals

1. Behaviour& Information Technology, Taylor & Francis
2. The Journal of Sustainable Product Design, Publisher: Springer
3. International Journal of Design; College of Design, National Taiwan University of Science and Technology, Taiwan.
4. Virtual & Physical Prototyping, Taylor & Francis

Magazines

1. 3) ID
2. 4) Form

Internet Sites

1. http://www.ulrich-eppinger.net/
2. http://www.npd-solutions.com
3. http://www.qfdi.org
4. http://www.cheshirehenbury.com/rapid/

Electronic Product Design Lab

1. Exercises on sketching and drawing, use of colors
2. Practice use of model making materials and processes
3. Practice methods and techniques of prototype making using sheet metal and plastic fabrication

Course Outcomes:

After completion of course the student shall be able to:

CO1: Design electronic products using user centered design process. (L5)

CO2: Develop sketches, virtual and physical appearance models to communicate proposed designs. (L3)

CO3: describe how perceptual set is influenced by an individual's characteristics and mental state. (L4)

CO4: Refine product design considering engineering design & manufacturing requirements and
constraints. (L2)

CO5: Make mock-up model and working prototype along with design documentation. (L6)

EDT704: MEMS AND APPLICATIONS

L T P C
3 0 0 3

Course Description:

Micro-electromechanical systems (MEMS) is a process technology used to create tiny integrated devices or systems that combine mechanical and electrical components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimeters. This course is designed to understand the introduction and design of MEMS and also its applications in various fields of engineering

Course Objectives:

- An outline of Microsystems and introduction to fabrication.
- Exposure to MEMS sensors working principles.
- In detail fabrication processes.
- Knowledge of different Packaging techniques for MEMS sensors.
- Application of MEMS devices across different area of engineering.

Module I **5 Hours**

Overview of MEMS and Microsystems: MEMS and Microsystems, Typical MEMS and Micro-system Products, Evolution of Micro- fabrication, Microsystems and Microelectronics, Microsystems and Miniaturization

Learning Outcomes:

After completion of this module, the student will be able to

- Differentiate the MEMS and Microsystems (L1).
- Explain about the evolution of MEMS (L1).
- Describe Miniaturization (L2).
- Illustrate the concepts of Microfabrication (L2).

Module II **8 Hours**

Working Principles of MEMS: Micro-sensors, Micro-actuation, MEMS with Micro-actuators, Micro-accelerometers, Micro- fluidics, MEMS for Thermal Sensors

Learning Outcomes:

After completion of this module, the student will be able to

- Understand the working principle of MEMS (L3)
- Analyze the Micro sensors and Micro Actuators (L3)
- Describe the working principles of MEMS applications (L3)
- Explore the MEMS as thermal sensors (L4)

Module III **10 Hours**

MEMS Fabrication Processes Photo-lithography, Ion Implantation, Diffusion, Oxidation, Chemical Vapor Deposition, Physical Vapour Deposition—Sputtering, Deposition by Epitaxy,

Etching, Summary of Micro-fabrication, Overview of Micro-manufacturing, Bulk Micro-manufacturing, Surface Micro-machining, The LIGA Process

Learning Outcomes:
After completion of this module, the student will be able to

- Describe the MEMS fabrication process (L2)
- Knows the step by step process of MEMS design (L3)
- Understand the various technologies that are involved in MEMS fabrication process (L2)
- Analyze the important of Micro manufacturing process (L3)

Module IV **12 Hours**

MEMS Packaging: Overview of Mechanical Packaging of Microelectronics, Micro-system Packaging, Interfaces in Micro-system Packaging, Essential Packaging Technologies, Three-Dimensional Packaging, Assembly of MEMS, Selection of Packaging Materials, Signal Mapping and Transduction, Design Case: Pressure Sensor Packaging

Learning Outcomes:
After completion of this module, the student will be able to

- Explain the importance of MEMS packaging (L1)
- Knows in detail about the MEMS packaging technologies (L3)
- Understand the various materials that are used in 3D design(L2)
- Analyze the importance of signal mapping and design case (L3)

Module V **10 Hours**

Applications of MEMS: Applications of MEMS in the Automotive Industry and Industrial Products. Case Studies of usage of MEMS Accelerometer, Proximity Sensor and Thermal Sensor

Learning Outcomes:
After completion of this module, the student will be able to

- Analyze the various applications of MEMS packaging (L3)
- Knows in detail about the MEMS case studies in various filed of application (L3)
- Understand the MEMS thermal, proximity and Accelerometer sensors (L2)
- Recall the design and application of MEMS in Industrial products (L1)

Text Books:

1. Tai-Ran Hsu, " MEMS and Microsystems: Design and Manufacture", Wiley, 2008.
2. N. Maluf, "An Introduction To Microelectromechanical Systems Engineering", 2nd Ed, Artech House,Inc, 2004.

References:

1. Gregory Kovacs, "Micromachined Transducers Sourcebook", WCB McGraw-Hill, Boston,1998.
2. S. Senturia, "Microsystem Design", Springer, 2001

3. M.-H. Bao, “Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes”, Elsevier, New York, 2000
4. J. Allen, "Micro Electro Mechanical System Design", CRC, 2005
5. M.J. Madou, "Fundamentals of Microfabrication",3rd Ed, CRC, 2011
6. V.K. Varadan, “Microstereolithography and other fabrication techniques for 3D MEMS”, Wiley, 2001.
7. Wolfgang Menz, “Microsytem technology”, Weinheim, Wiley-VCH, 2001
8. Gabriel M. Rebeiz Hoboken, “RF MEMS: theory, design and technology”, Wiley, 2003

Course Outcomes:

After completion of course the student shall be able to:

1. Understand the field of Micro systems (L1)
2. Gain the knowledge of MEMS fabrication process (L2)
3. Analyze the MEMS fabrication processes (L3)
4. Evaluate the different packaging techniques of Microsystems (L2)
5. Apply MEMS sensors to various fields of engineering (L1)

EDT706: DESIGN FOR QUALITY AND RELIABILITY

L T P C
3 0 0 3

Module I **9 Hours**

Introduction and Process Control for Variables: Introduction, definition of quality, basic concept of quality, definition of SQC, benefits and limitation of SQC, Quality assurance, Quality cost, variation in process, factors, process capability, process capability studies and simple problems, Theory of control chart, uses of control chart, Control chart for variables, X chart, R chart and s chart.

Module II **9 Hours**

Process Control for Attributes: Control chart for attributes, control chart for proportion or fraction defectives, p chart and np chart, control chart for defects, C and U charts, State of control and process out of control identification in charts.

Module III **9 Hours**

Acceptance Sampling: Lot by lot sampling, types, probability of acceptance in single, double, multiple sampling techniques, O.C. curves, producer's Risk and consumer's Risk. AQL, LTPD, AOQL concepts, standard sampling plans for AQL and LTPD, uses of standard sampling plans.

Module IV **9 Hours**

Life Testing–Reliability: Life testing, Objective, failure data analysis, Mean failure rate, mean time to failure, mean time between failure, hazard rate, system reliability, series, parallel and mixed configuration, simple problems. Maintainability and availability, simple problems. Acceptance sampling based on reliability test, O.C Curves.

Module V **9 Hours**

Quality and Reliability: Reliability improvements, techniques, use of Pareto analysis, design for reliability, redundancy unit and standby redundancy, failure and survival probability; hazard rate, conditional probability and multiplication rules, component and system reliability and its prediction; failure mode and fault tree analysis, reliability testing. Optimization in reliability, Product design, Product analysis, Product development, Product life cycles.

Text Books

1. Grant, Eugene. L, "Statistical Quality Control ", McGraw-Hill, 1996
2. L. S. Srinath, "Reliability Engineering" Affiliated East West Press, 1991
3. R. C. Gupta, "Statistical Quality control", Khanna Publishers, 1997
4. Besterfield D.H., "Quality Control", Prentice Hall, 1993
5. Sharma S.C., "Inspection Quality Control and Reliability", Khanna Publishers, 1998
6. Connor, P.D.T.O., "Practical Reliability Engineering", John Wiley, 1993
7. Montgomery, D.C., "Introduction to Statistical Quality Control", 5/e, John Wiley & Sons, 2005.
8. Garvin, D.A, "Managing Quality: Strategic and Competitive Edge", The Free Press, 1989.
9. K C Jain, A K Chitale, "Quality Assurance and Total Quality Management", Khanna Publishers, 2001.
10. M. Mahajan, "Statistical Quality Control", Dhanpat Rai & Co. (P) Ltd., 2002.
11. B. L. Hanson, P. M. Ghare, "Quality Control & Application", Prentice Hall of India, 1987.

12. Total Quality Management, Dale H. Besterfield, Carol Besterfield-Michna, Glen H. Besterfield and Mary Besterfield-Sacre, Pearson Education, 2011.
13. S. Kumar, “Total Quality Management”, Laxmi Publication Pvt. Ltd., 2006.
14. Srinath L. S., “Reliability Engineering” , Affiliated East West Press, 2002.
15. K C Arora, “Total Quality Management”, S K Kataria & Sons, 2009
16. Eugene L. Grant and Richard S. Leavenworth, “Statistical Quality Control”, Tata McGraw-Hill Publishing Company Ltd., 1999.
17. Poornima M. Charantimath, “Total Quality Management”, Pearson Education, 2005
18. N. Logothetis, “Managing for Total Quality”, Prentice Hall of India Pvt. Ltd., 1992.
19. John M. Nicholas, “Competitive Manufacturing Management”, Mcgraw Hill, 2001.
20. Barrie G. Dole, “Managing Quality”, Blackwell Publishing, 2002.
21. Samunel K Ho, “Total Quality Management - An Integrated Approach”, Crest Publishing House, 1999.
22. I. R. Miller, J. E. Freund & R. Johnson, “Probability and Statistics for Engineers”, Prentice Hall of India, 2017.
23. P. A. Tobias, D. C. Trindade, “Applied Reliability”, 3/e, Chapman and Hall/CRC, 2011.
24. W. Q. Meeker, Luis A. Escobar, “Statistical Methods for Reliability Data” Wiley Interscience, 1998
25. W. Nelson, “Applied Life Data Analysis”, Wiley, New York, 1982.
26. W. Nelson, “Accelerated Testing”, Wiley, New York, 1990.

Links

1. International Technology Roadmap for Semiconductors JEDEC Sematech
2. NIST Engineering Statistics Handbook.

Reference Books

1. Weibull, Waloddi, “A Statistical Distribution of Wide Applicability”, Journal of Applied Mechanics, 1951, pp. 293-297.
2. P. Nigh, W.Needham, K. M. Butler, P. C. Maxwell, R. C. Aitken, "An Experimental Study Comparing the Relative Effectiveness of Functional Scan, Iddq, and Delay Fault Testing," 15th IEEE VLSI Test Symposium 1997, pp 459-464.

EDT742: IC MANUFACTURING

L T P C
3 1 0 4

This course familiarizes the students with automation principles and its strategies, NMOS, CMOS technology, physical simulation and TCAD, Process simulation, Binomial, Poisson yield models, yield prediction based on critical area extraction, defect-fault relationship, Visualization of device physical operation and Technology optimization through process variation.

Course Objectives

- To Introduce the fundamental concepts of manufacturing and automation in production.
- To study the different semiconductor IC technologies and familiarize with TCAD simulation tool.
- To provide an understanding on yield modeling and analysis in application for Design for Manufacturability.
- To describe layout driven fault analysis techniques.
- To understand the device physical models, Numerical algorithms, solutions and device performance optimization and trade-offs.

Module I **9 Hours**

Fundamentals of Manufacturing: Production systems, automation principles and its strategies; Manufacturing industries; Types of production function in manufacturing.

Learning Outcomes:
After completion of this unit, the student will be able to

explain production systems(L2)
demonstrate the automation principles and its strategies (L2)
describe the types of function in manufacturing. (L2)

Module II **9 Hours**

Semiconductor technology: Wafer process, NMOS, CMOS technology, acceptable regions, process disturbances, experimental planning and project evaluation. Introduction to physical simulation and TCAD. Basic semiconductor processing steps such as implantation, diffusion, oxidation. Design of experiment and wafer split, Process simulation and BJT and CMOS process flow

Learning Outcomes:
After completion of this unit, the student will be able to

summarize the different semiconductor IC technologies. (L2)
outline the TCAD simulation tool. (L2)
explain semiconductor processing steps implantation, diffusion and oxidation. (L2)
illustrate the design of experiment and wafer split and process simulation. (L3)
distinguish between BJT and CMOS process flow. (L4)

Module III **9 Hours**

Functional Yield: Yield economics, manufacture and design strategies. Binomial, Poisson yield models, defect density, redundancy, Layout defect-sensitivity: Spot defects and their size distributions, Probabilistic analysis, susceptible sites, single-layer critical areas, yield prediction based on critical area extraction

Learning Outcomes:
After completion of this unit, the student will be able to

summarize yield economics, manufacture and design strategies (L2)
analyze the yield models. (L5)
understand the yield prediction based on critical area extraction. (L5)

Module IV **9 Hours**

Layout Driven fault analysis: Technology and defect semantics, defect-fault relationship, multiple –layer critical areas, realistic fault extraction.

Learning Outcomes:
After completion of this unit, the student will be able to

explain technology and defect semantics. (L2)
illustrate defect-fault relationship and multiple –layer critical areas (L3)
understand the realistic fault extraction. (L5)

Module V **9 Hours**

Virtual Device Simulation: Device physical models. Numerical algorithms and solutions. Device simulation and electrical characterization. Device structural and electrical parameters. Visualization of device physical operation. Integration Module: Virtual Process Integration Device/process target-variable relations. Technology optimization through process variation. Device performance optimization and trade-offs.

Learning Outcomes:
After completion of this unit, the student will be able to

describe numerical algorithms, device simulation and electrical characterization (L3)
analyze visualization of device physical operation.(L5)
understand virtual process integration device/process target-variable relations.(L5)

Text Books:

1. S. M. Sze Streetman," VLSI Technology", McGraw Hill Publications, 2003.
2. C.Y. Chang and S.M. Sze (Ed), "ULSI Technology", McGraw-Hill Companies Inc., 1996.
3. S. K. Gandhi, "VLSI fabrication Principles" ,John Wiley Inc., New York, 1983.
4. Sorab K. Gandhi, "The Theory and Practice of Microelectronics", John Wiley & Sons, 1968.

References:

1. B.G Streetman, "VLSI Technology", Prentice Hall, 1990.
2. A.S Grove, "Physics and Technology of Semiconductor Devices", John Wiley & Sons, 1967

3. J Talavage, R.G. Hannam, “Flexible Manufacturing Systems in Practice”, Marcell Decker, 1987.
4. Pandley P.S., Shah. N., “Modern Manufacturing Processes”, 1980.
5. Marc J. Madou, Fundamentals of Micro-Fabrication: The Science of Miniaturization, 2/e, CRC Press, 2006

Course Outcomes:

After successful completion of the course, the student will be able to

- analyze the fundamental concepts of manufacturing and automation in production. (L5)
- study the different semiconductor IC technologies and familiarize with TCAD simulation tool. (L2)
- understand on yield modeling and analysis in application for Design for Manufacturability. |(L5)
- describe layout driven fault analysis techniques. (L3)
- understand the device physical models, Numerical algorithms, solutions and device performance optimization and trade-offs. (L5)

EDT744: ADVANCED DIGITAL SIGNAL PROCESSING

L T P C
3 1 0 4

Module I **9 Hours**

Digital Processing of Continuous Signals, Discrete time Signals and Systems, Characterization of Discrete LTI Systems, Correlation of Signals and Random Signals. Continuous Time Fourier Transform, Discrete Time Fourier Transform, Fourier Series, Discrete Fourier Transform, Fast Fourier Transform. Z-transforms, Calculation of frequency and Phase response. Digital Filters, recursive and non-recursive filters, order and coefficients of digital filter, stability, transfer function. Realization of IIR and FIR filters, Filter design, Design of Lowpass, Highpass, Bandpass and Bandstop IIR and FIR Filters.

Module II **9 Hours**

Concepts of Multirate Digital Signal Processing, Design of practical sampling rate converters, Implementation of sampling rate converters - decimators, Implementation of interpolators, Sample rate conversion using poly-phase filter structure. Application examples: High quality Analog to Digital conversion for Digital Audio, Efficient Digital to Analog conversion in compact hi-fi systems, Application in the acquisition of High- Quality data, Multirate narrowband digital filtering, High resolution narrowband spectral analysis.

Module III **9 Hours**

Introduction and evolution of Digital Signal Processors, Computer Architecture of DSP – Harvard and Modified Harvard Architecture, VLIW, Super scalar, pipelining, Multiplier and Accumulator (MAC), Special Instructions, On-Chip memory Cache, Special Purpose DSP Hardware, Fixed and Floating point Digital Signal Processors. DSP System Design – Algorithm Development, Selection of DSP Hardware, Software development, Software Development tools.

Module IV **9 Hours**

Case Study of a Fixed Point Digital Signal Processor (TMS320C55xx) – Architecture, overview, On-chip memory, memory mapped registers, Buses, peripherals, addressing modes, Assembly language, Mixed C and Assembly language programming.

Module V **9 Hours**

Implementation of Algorithms on Digital Signal Processors (TMS320C55xx): FIR Digital Filtering, IIR Digital Filtering, FFT Processing, Adaptive Filtering. DSP Applications: Adaptive removal of Ocular Artefacts from human EEGs, Equalization of digital audio signals.

Text Books:

1. S.K. Mitra, “Digital Signal Processing: A Computer Based Approach”, 4/e, McGraw Hill Education, 2013
2. Emmanuel C.Ifeachor and Barrie W. Jervis, “Digital Signal Processing: A Practical Approach”, 2/e, Prentice Hall, 2001

References:

1. John G. Proakis, Dimitris G Manolakis, “Digital Signal Processing: Principles, Algorithms and Applications”, 4/e, Pearson Education, 2007.
2. Ashok Ambardar, “Digital Signal Processing: A Modern Introduction, 1/e, Nelson Engineering, 2007.
3. Steven W.Smith, “The Scientist and Engineer's Guide to Digital Signal Processing, 1/e, California Technical Publication, 1998.
4. B. Venkataramani, M. Bhaskar, “Digital Signal Processors: Architecture, Programming and Applications, 2/e, Tata Mc graw-Hill Education Private Limited, 2011.
5. CPU reference guide, Mnemonics and Instruction set reference guide.
6. NPTEL video lecture on Digital Signal Processing: http://nptel.ac.in/courses/117102060/

EDT746: MIXED SIGNAL DESIGN

L T P C
3 1 0 4

Course objectives

- To understand A/D and D/A conversion process.
- To design analog and digital filters as per the given specifications.
- To design D/A converter as per the specifications.
- To design A/D converter as per the specifications.
- To understand interconnects and phase locked loop and design of phase locked loop as per specifications.

Module I **10 Hours**

Introduction to A/D and D/A conversion: Analog and discrete-time signal processing, introduction to sampling theory, quantization, quantization noise, aliasing and reconstruction filtering. Sample and Hold characteristics, DAC and ADC specifications

Module II **10 Hours**

Analog and Digital Filters: Analog continuous-time filters: passive and active filters Basics of analog discrete-time filters and Z-transform Switched-capacitor filters, Non-idealities in switched-capacitor filters. Switched- capacitor filter architectures, Switched-capacitor filter applications

Module III **8 Hours**

Analog to digital converters (ADC): Basics of data converters. Nyquist rate A/D converters, Successive approximation ADCs, Dual slope ADCs, Flash ADC, Pipeline ADC, Hybrid ADC structures., Two step ADC, Interpolating ADC, Folding ADC, Time Interleaved ADC, High-resolution ADC

Module IV **8 Hours**

Digital to analog converters (DAC): Nyquist rate D/A converters, Decoder based converters, Binary scaled converters, R-2R ladder networks, Thermometer code converters, Hybrid converters, current steering, charge scaling DACS, pipelined DACs, Oversampling Converters.

Module V **9 Hours**

Interconnects and PLL: Interconnects and data transmission., Voltage-mode signaling and data transmission., Current-mode signaling and data transmission., Basics of PLL., Analog PLL, Digital PLL, Delay locked loops, PLLs with charge pump, phase comparators, Dynamics of PLL.

Text Books

1. R. Jacob Baker, “CMOS Mixed-Signal Circuit Design”, 3/e, Wiley India, IEEE Press, reprint, 2014.
2. David A. Johns, Ken Martin, “Analog Integrated Circuit Design”, 2/e, Oxford University Press, 2010.

References

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, 2/e, Tata-Mc GrawHill, 2017.
2. Phillip E.Allen, Douglas R. Holberg, “CMOS Analog Circuit Design”, 3/e, Oxford University Press, 2013.
3. Mikael Gustavsson, J. Jacob Wikner, Nianxiong Nick Tan, “CMOS Data Converters for Communications”, 1/e, Springer, 2010.

EDT748: MANUFACTURING ENGINEERING

L T P C
3 1 0 4

Course Outcomes:

1. To understand the basic principles and tools needed for design for manufacturing (DFM).
2. Student able to understand the role of important factors required for form design in case of DFM mainly welding and forging.
3. Student able to understand design aspects of sheet metal fabrication.
4. Student able to understand the role of important factors required for form design in case of DFM.
5. Student able to understand the importance for various forms of vacuum forming and product life cycle of rapid prototyping in modern era.

Module I **9 Hours**

Introduction: General design principles for manufacturability, Factors influencing design, Systematic working plan for the designer, Types of problems to be solved-Possible solutions, Evaluation method, Process capability , Feature tolerances , Geometric tolerances ,Assembly limits, Datum features , Tolerance stacks, Interchangeable part manufacture and selective assembly.

Learning Outcomes:
After completion of this module, the student will be able to

- understand the concept of design principles (L1)
- illustrate about the systematic working plan for the designer (L1)
- describe types of problems for possible solutions (L2)
- illustrate different features of design principles required for manufacturing (L2)

Module II **9 Hours**

Factors Influencing Form Design: Materials choice - Influence of basic design, mechanical loading, material, production method, size and weight on form design- form design of welded members and forgings.

Learning Outcomes:
After completion of this module, the student will be able to

- understand the concept of material selection for manufacturing (L1)
- illustrate about the mechanical loading, production method etc. (L1)
- describe role of size and weight on form design (L2)
- illustrate different form designs required for welded and forging elements (L2)

Module III **9 Hours**

CAD Designs: Definition of CAD Tools, Types of system, CAD/CAM system evaluation Criteria, Graphics standards, functional areas of CAD, Modeling and viewing, software documentation, efficient use of CAD software. Wire frame modeling -Types of mathematical representation of curves, wire frame models, wire frame entities, parametric

representation of synthetic curves – Hermite cubic splines, Bezier curves, B-Splines, rational curves – NURBS.

Learning Outcomes:
After completion of this module, the student will be able to

- understand the role of computer in manufacturing, more specifically required at its design stage (L1)
- illustrate efficient use of CAD software (L1)
- describe the concept of wire frame modelling used in CAD (L2)
- illustrate different parametric representation of synthetic curves (L2)

Module IV **9 Hours**

Sheet Metal Fabrication: Sheet Metal Fitting Layout & Design, bending, bending angle, Sheet Metal Fitting Fabrication, Sheet Metal Drafting & Blueprint Reading, Sheet Metal Welding, Sheet Metal Practical Problem Solving, surface finishes, Powder coating.

Learning Outcomes:
After completion of this module, the student will be able to

- understand the concept of sheet metal fabrication (L1)
- illustrate fitting layout and design aspects of sheet metal (L1)
- describe the concept sheet metal drafting and blueprint reading (L2)
- understand the concept of sheet metal welding, powder coating etc. (L1)

Module V **9 Hours**

Vacuum Forming: Introduction to Thermoforming, General Forming Concepts, Vacuum Forming process, creating a thermoformed model using vacuum forming. **Rapid Prototyping** Rapid Product Development (RPD), Product Development Cycle, Detail design, Prototype and tooling. RAPID PROTOTYPING (RP): Principle of RP technologies and their classification of RP systems, Stereo lithography systems, Selection of RP process; Issues in RP; Emerging trends, Direct Metal Laser Sintering (DMLS) system, Principle, process parameters, process details, Applications.

Learning Outcomes:
After completion of this module, the student will be able to

- understand the concept forming in manufacturing engineering (L1)
- illustrate different aspects of vacuum forming (L1)
- describe the concept rapid prototyping (RP) in manufacturing engineering (L2)
- understand the concept of direct metal laser sintering (DMLS), as part of the emerging trends in RP (L1)

Text Books

1. Bralla, “Design for Manufacture Handbook”, McGraw Hill, 1999.
2. Boothroyd, G, Heartz, Nike, “Product Design for Manufacture”, Marcel Dekker, 1994.
3. Marciniak,Z., Duncan J.L., Hu S.J., ‘Mechanics of Sheet Metal Forming’, Butterworth- Heinemann, Elsevier, 2006.

4. Llbrahim Zeid "CAD/CAM Theory and Practice", McGraw Hill International, 1991.
5. Chua Chee Kai, Leong Kah Fai, "Rapid Protoyping: Principles and Applications in Manufacturing", John Wiley and Sons, 1997.
6. Martin Helander, A Guide to the Ergonomics of Manufacturing, East West Press, 1996

References

1. Boothroyd G., "Design for Assembly Automation and Product Design", New York, Marcel Dekker, 1980.
1. Bralla, "Design for Manufacture Handbook", McGraw hill, 1999.
2. Boothroyd, G, Heartz and Nike, "Product Design for Manufacture", Marcel Dekker, 1994.
3. Kevien Otto and Kristin Wood, "Product Design", Pearson Publication, 2004.
4. I.N.G. Robert Matouslk, "Engineering Design", Blackie & Sons Limited, 1962.
5. Harry peck, "Designing for Manufacture", Pitman Publishing, 1973
6. D.E. Walsh, "Do It Yourself Vacuum Forming for the Hobbyist, Workshop Publishing", Lake Orion, MI, 2002
7. P. N. Rao, "CAD/CAM", Tata McGraw Hill Publications, 2010
8. Paul F. Jacobs, "Stereo Lithography and other RP & M Technologies: from Rapid Prototyping to Rapid Tooling", SME/ASME, 1996
1. D. Faux, M. J. Pratt, "Computational Geometry for Design and Manufacture", John Wiley and Sons, 1979.
2. Pham, D.T., Dimov.S.S., "Rapid Manufacturing", Springer-Verlag, London, 2001.
3. Altan T., "Metal forming: Fundamentals and applications", American Society of Metals, Metals Park, 2003.
4. E.J. Mc Cormic, "Human factors in Engineering Design", McGraw Hill, 1976.

EDT792: TECHNICAL SEMINAR

L	T	P	C
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Two technical seminars are to be presented by each student in any of the following areas

- Manufacturing and Design
- Low Power Circuit Design
- Analog Integrated Circuit Design
- Semiconductor Device Modeling and Simulation
- Advanced Digital System Design
- RF Systems Design
- EMI/EMC in Electronic Systems
- IC Manufacturing
- Advanced Embedded Systems Design
- Advanced Digital Signal Processing
- Industrial Design of Electronic Products
- Mixed Signal Design
- MEMS and Applications
- Manufacturing Engineering
- Design for Quality and Reliability

EDT891: PROJECT WORK AND SEMINAR I

L	T	P	C
0	0	0	8

Project guide allotment, student guidance and evaluation of the Project Work will be carried out by CDAC, Hyderabad in association with the internal guide at GITAM (at respective campus)

EDT892: PROJECT WORK AND SEMINAR II

L	T	P	C
0	0	0	12

Project guide allotment, student guidance and evaluation of the Project Work will be carried out by CDAC, Hyderabad in association with the internal guide at GITAM (at respective campus)